We claim:

We claim:

1. A machine-readable medium that provides instruction, which when executed by a set of processors, cause said set of processors to perform operations comprising:

receiving a plurality of signals at a first clock rate;

synchronizing the plurality of signals to a second clock rate; and

deframing the plurality of signals.

2. The machine-readable medium of claim 1 wherein the second clock rate is greater than twice the first clock rate.

3. The machine-readable medium of claim 1 wherein synchronizing the plurality of signals comprises adding a set of stuffing bits to the plurality of signals.

4. The machine-readable medium of claim 1 wherein the deframing the plurality of signals comprises:

cycling through each of the plurality of signals; and

deframing each of the plurality of signals in a cycle.

5. A machine-readable medium that provides instruction, which when executed by a set of processors, cause said set of processors to perform operations comprising:

receiving a first and second signal at a first and second clock rate;

multiplexing the first and second signal; and

deframing the multiplexed first and second signal.

6. The machine-readable medium of claim 5 wherein the first and second clock rate are the same clock rate.

7. The machine-readable medium of claim 5 wherein the multiplexing is in accordance with a third clock rate, the third clock rate being greater than the sum of the first and second clock rate.

8. The machine-readable medium of claim 5 further comprising synchronizing the first and second signal to a third clock rate before multiplexing the first and second signal.

9. A machine-readable medium that provides instruction, which when executed by a set of processors, cause said set of processors to perform operations comprising:

receiving a first signal at a first rate;

receiving a second signal at a second rate;

synchronizing the first and second signal to a third rate;

multiplexing the synchronized first and second signal; and

deframing the multiplexed first and second signal.

10. The machine-readable medium of claim 9 wherein the first rate and the second rate are approximately equal, a sum of the first and second rate being less than the third rate.

11. The machine-readable medium of claim 9 wherein the third rate is faster than the sum of the first and second rate.

12. The machine-readable medium of claim 9 wherein the synchronizing the first and second signal comprises adding a set of stuffing bits to the first and second signal.

13. An apparatus comprising:

a first and second receiving unit to receive a first and second signal;

a multiplexing unit coupled to the first and second receiving unit, the multiplexing unit to multiplex the first and second signal;

a deframing unit coupled to the multiplexing unit, the deframing unit to deframe the multiplexed first and second signal from a format.

14. The apparatus of claim 13 wherein the first and second signals are received at a first and second rate.

15. The apparatus of claim 13 wherein the first and second signals are received at a first rate.

16. The apparatus of claim 13 further comprising:

a domain clock to transmit a clock signal;

the first and second receiving unit coupled to the domain clock, the first and second receiving unit to synchronize the first and second signal to the clock signal, the domain clock being faster than a sum of a first rate of the first signal and a second rate of the second signal.

17. The apparatus of claim 13 further comprising:

a selecting unit coupled to the deframing unit, the selecting unit to select either the first or second signal and to transmit the selected first or second signal;

a second multiplexing unit coupled to the selecting unit, the multiplexing unit to multiplex the selected first or second signal and a third signal;

a third receiving unit coupled to the second multiplexing unit, the third receiving unit to receive the third signal and transmit the third signal to the second multiplexing unit;

a second deframing unit coupled to the multiplexing unit, the second deframing unit to deframe the multiplexed third signal and the selected first or second signal from a second format.

18. An apparatus comprising:

a domain clock to transmit a clock signal;

a first and second receiving unit coupled to the domain clock, the first and second receiving unit to receive a first and second signal and to synchronize the first and second signal to the clock signal;

a multiplexing unit coupled to the first and second receiving unit, the multiplexing unit to multiplex the synchronized first and second signal; and

a deframing unit coupled to the multiplexing unit, the deframing unit to deframe the multiplexed first and second signal from a format.

19. The apparatus of claim 18 wherein the first and second signals are received at a second and third clock rate, the sum of the second and third clock rate being less than a rate of the clock signal.

20. The apparatus of claim 18 wherein to synchronize the first and second signal comprises adding a set of stuffing bits to the first and second signal.

21. The apparatus of claim 18 wherein the clock signal's rate is greater than a sum of the first and second signal's rate.

22. The apparatus of claim 18 further comprising:

a selecting unit coupled to the deframing unit, the selecting unit to select either the first or second signal and to transmit the selected first or second signal;

a second multiplexing unit coupled to the selecting unit, the multiplexing unit to multiplex the selected first or second signal and a third signal;

a third receiving unit coupled to the second multiplexing unit, the third receiving unit to receive the third signal and transmit the third signal to the second multiplexing unit;

a second deframing unit coupled to the multiplexing unit, the second deframing unit to deframe the multiplexed third signal and the selected first or second signal from a second format.

23. An apparatus comprising:

a domain clock to transmit a clock signal;

a receiving unit coupled to the domain clock, the receiving unit to receive a data signal and to synchronize the data signal to the clock signal, the data signal having a plurality of channels;

a first deframing unit coupled to the receiving unit, the first deframing unit to deframe the data signal from a format and to identify the plurality of channels; and

a second deframing unit coupled to the first deframing unit, the second deframing unit to cycle through each of the plurality of channels to deframe from a second format.

24. The apparatus of claim 23 wherein the clock signal is faster than the data signal.

25. The apparatus of claim 23 wherein to synchronize the data signal comprises adding a set of stuffing bits to the data signal.

26. The apparatus of claim 23 further comprising:

a second receiving unit coupled to the domain clock, the second receiving unit to receive a second data signal and to synchronize the second data signal to the clock signal;

a multiplexing unit coupled to the first deframing unit and the second receiving unit, the multiplexing unit to multiplex the deframed data signal and the synchronized second data signal; and

the second deframing unit coupled to the multiplexing unit, the second deframing unit to alternate between deframing the plurality of channels and deframing the second data signal.

27. An apparatus comprising:

a domain clock to transmit a clock signal;

a first and second receiving unit coupled to the domain clock, the first and second receiving unit to receive a first and second signal and to synchronize the first and second signal to the clock signal;

a multiplexing unit coupled to the first and second receiving unit, the multiplexing unit to multiplex the synchronized first and second signal;

a first deframing unit coupled to the multiplexing unit, the first deframing unit to deframe the multiplexed first and second signal from a first format; and

a second deframing unit coupled to the first deframing unit, the second deframing unit to deframe the multiplexed first and second signal from a second format.

28. The apparatus of claim 27 wherein the first and second signals are transmitted at a first and second rate, the clock signal's rate being greater than a sum of the first and second rate.

29. The apparatus of claim 27 wherein the clock signal's rate is greater than a sum of the rate of the first and second signal.

30. The apparatus of claim 27 wherein to synchronize the first and second signal comprises adding a set of stuffing bits to the first and second signal.

31. An apparatus comprising:

a domain clock to transmit a clock signal;

a first receiving unit coupled to the domain clock, the first receiving unit to receive a first signal at a first rate and to synchronize the first signal to the clock signal;

a second receiving unit coupled to the domain clock, the second receiving unit to receive a second signal at a second rate and to synchronize the second signal to the clock signal;

a first deframing unit coupled to the first receiving unit, the first deframing unit to deframe the first signal from a first format;

a multiplexing unit coupled to the first deframing unit and the second receiving unit, the multiplexing unit to multiplex the deframed first signal and the second signal; and

a second deframing unit coupled to the multiplexing unit, the second deframing unit to deframe the multiplexed deframed first signal and the second signal from a second format.

32. The apparatus of claim 31 wherein the clock signal's rate is greater than a sum of the first and second rate.

33. The apparatus of claim 31 wherein the second signal is a set of signals.

34. The apparatus of claim 31 wherein the synchronize the first and second signal comprises adding a set of stuffing bits to the first and second signal.

35. A computer implemented method comprising:
receiving a plurality of signals at a first clock rate;
synchronizing the plurality of signals to a second clock rate; and
deframing the plurality of signals.

36. The computer implemented method of claim 35 wherein the second clock rate is greater than twice the first clock rate.

37. The computer implemented method of claim 35 wherein synchronizing the plurality of signals comprises adding a set of stuffing bits to the plurality of signals.

38. The computer implemented method of claim 35 wherein the deframing the plurality of signals comprises:
cycling through each of the plurality of signals; and
deframing each of the plurality of signals in a cycle.

39. A computer implemented method comprising:
receiving a first and second signal at a first and second clock rate;
multiplexing the first and second signal; and
deframing the multiplexed first and second signal.

40. The computer implemented method of claim 39 wherein the first and second clock rate are the same clock rate.

41 The computer implemented method of claim 39 wherein the multiplexing is in accordance with a third clock rate, the third clock rate being greater than the sum of the first and second clock rate.

42. The computer implemented method of claim 39 further comprising synchronizing the first and second signal to a third clock rate before multiplexing the first and second signal.

43. A computer implemented method comprising:

receiving a first signal at a first rate;

receiving a second signal at a second rate;

synchronizing the first and second signal to a third rate;

multiplexing the synchronized first and second signal; and

deframing the multiplexed first and second signal.

44. The computer implemented method of claim 43 wherein the first rate and the second rate are approximately equal, a sum of the first and second rate being less than the third rate.

45. The computer implemented method of claim 43 wherein the third rate is faster than the sum of the first and second rate.

46. The computer implemented method of claim 43 wherein the synchronizing the first and second signal comprises adding a set of stuffing bits to the first and second signal.